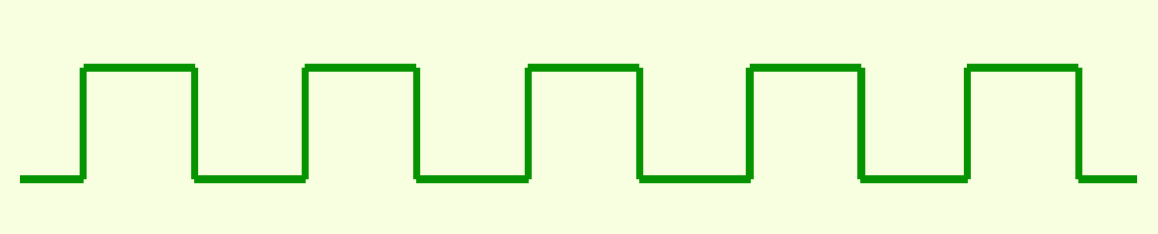
3.6 Sequential Circuits

- Combinational logic circuits are perfect for situations when we require the immediate application of a Boolean function to a set of inputs.
- However, when we need a circuit to change its value with consideration to its current state as well as its inputs.
  - These circuits have to "remember" their current state.
- *Sequential logic circuits* provide this functionality for us.

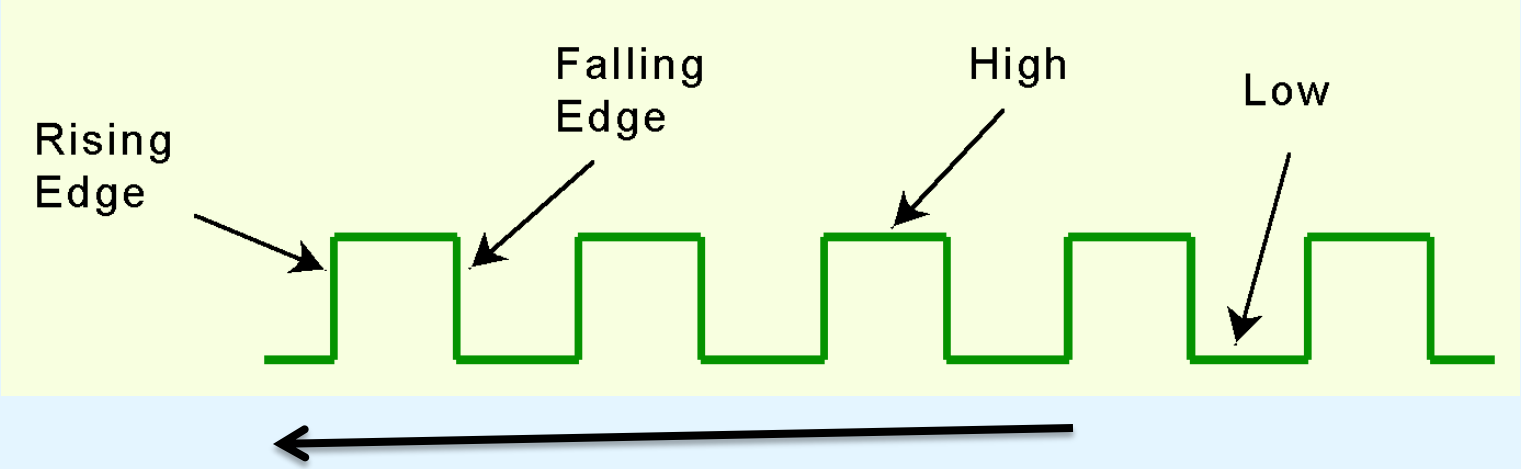
3.6 Sequential Circuits

- As the name implies, **sequential logic circuits** require a means by which **events can be sequenced**.
- State changes are controlled by clocks.
  - A "clock" is a special circuit that sends electrical pulses through a circuit.
- Clocks produce electrical waveforms such as the one shown below.



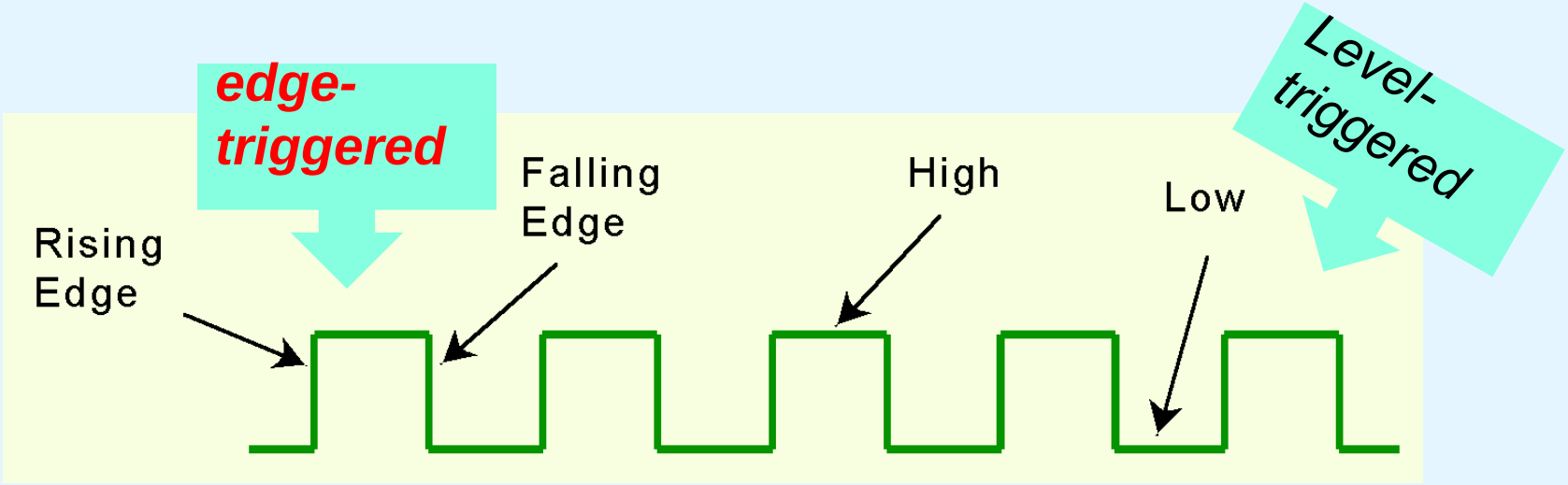
3.6 Sequential Circuits

- State changes occur in sequential circuits only when the clock ticks.
- Circuits can change state on the rising edge, falling edge, or when the clock pulse reaches its highest voltage.



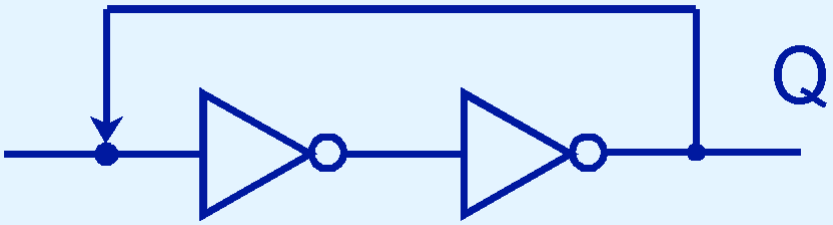
3.6 Sequential Circuits

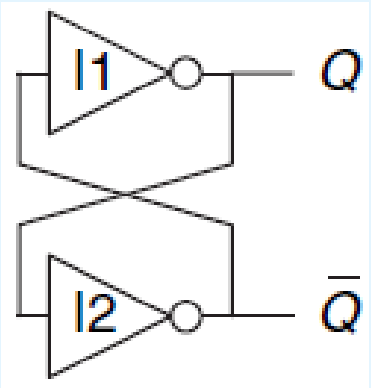
- Circuits that change state on the rising edge, or falling edge of the clock pulse are called ***edge-triggered.***
- *Level-triggered circuits* change state when the clock voltage reaches its highest or lowest level.



3.6 Sequential Circuits

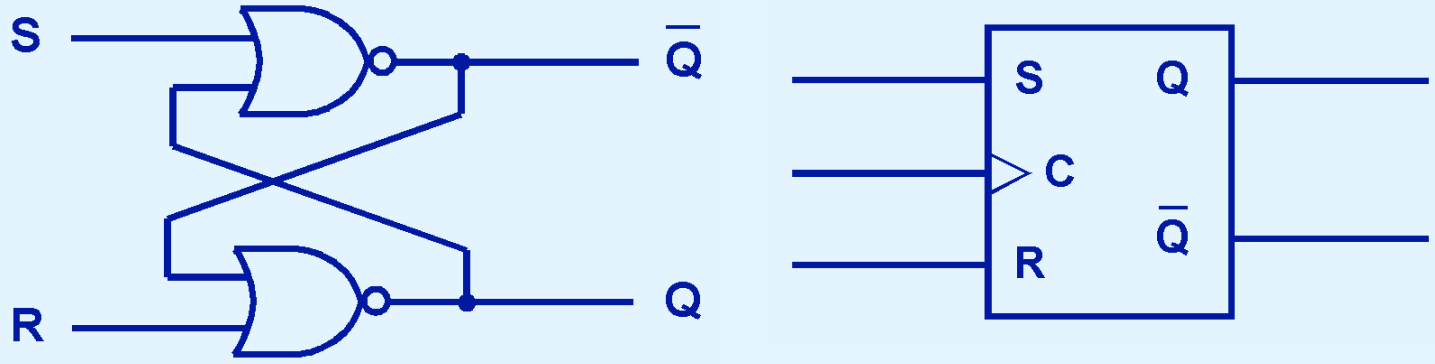
- To retain their state values, sequential circuits rely on *feedback.*
- Feedback in digital circuits occurs when an output is looped back to the input.
- A simple example of this concept is shown below.
  - If Q is 0 it will always be 0,
  - if it is 1, it will always be 1.
  - Why?





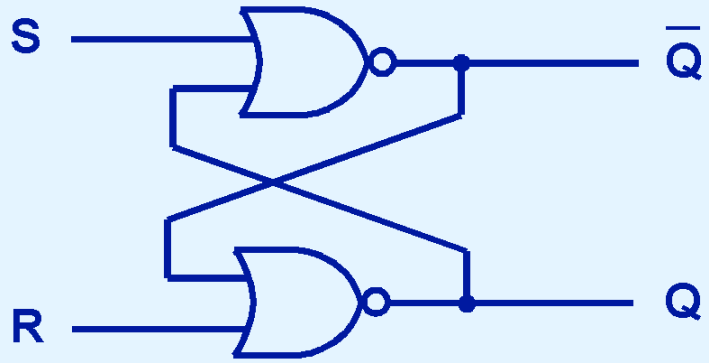
3.6 Sequential Circuits

- You can see how feedback works by examining the most basic sequential logic components, the SR Latch.
  - The "SR" stands for set/reset.
- The internals of an SR latch are shown below, along with its block diagram.



3.6 Sequential Circuits

- The behavior of an SR flip-flop is described by a characteristic table.
- Q(t) means the value of the output at time t. Q(t+1) is the value of Q after the next clock pulse.



S	R	Q(t+1)
0	0	Q(t) (no change)
0	1	0 (reset to 0)
1	0	1 (set to 1)
1	1	undefined

RS- Latch

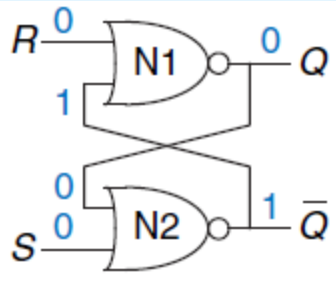


Figure (a)

Case Q= 0

Because S and Q are FALSE, N2 produces a TRUE output on Q, as shown in Figure (a). Now N1 receives one TRUE input, Q, so its output, Q, is FALSE, just as we had assumed.

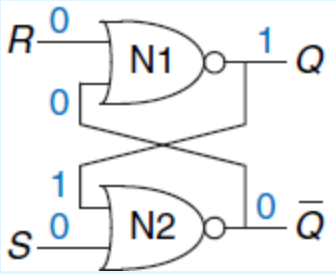
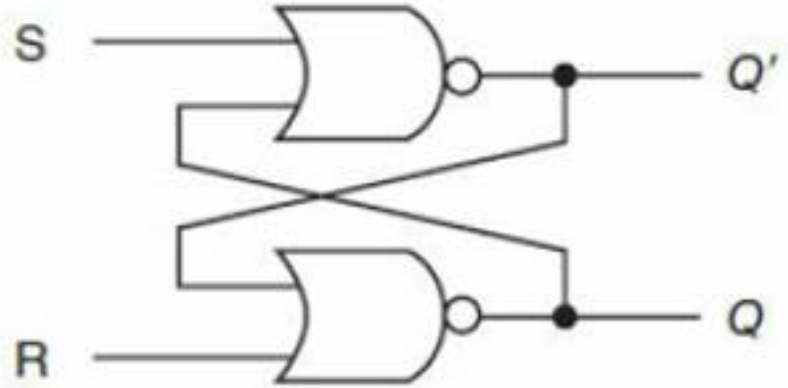


Figure (b)

Case Q= 1

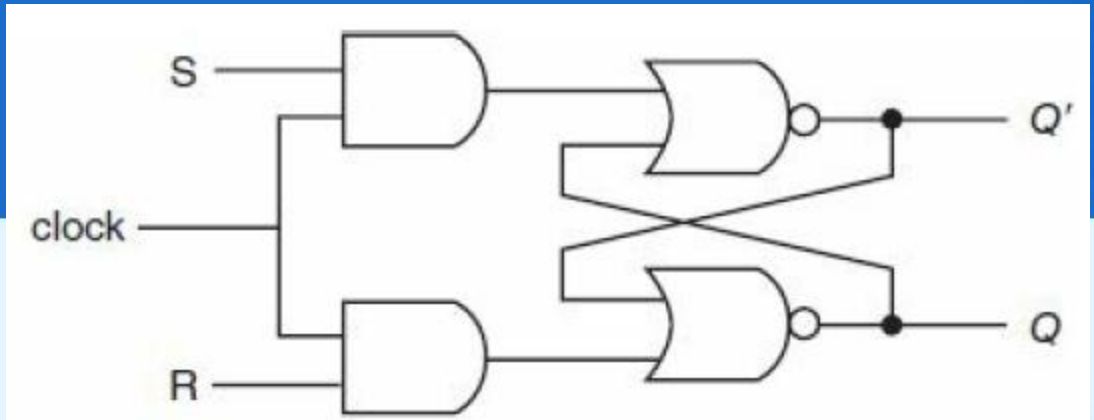
Because Q is TRUE, N2 produces a FALSE output on Q, as shown in Figure (b). Now N1 receives two FALSE inputs, R and Q, so its output, Q, is TRUE, just as we had assumed.

When R and S are 0, Q will remember this old value, Q(t). This circuit has memory.

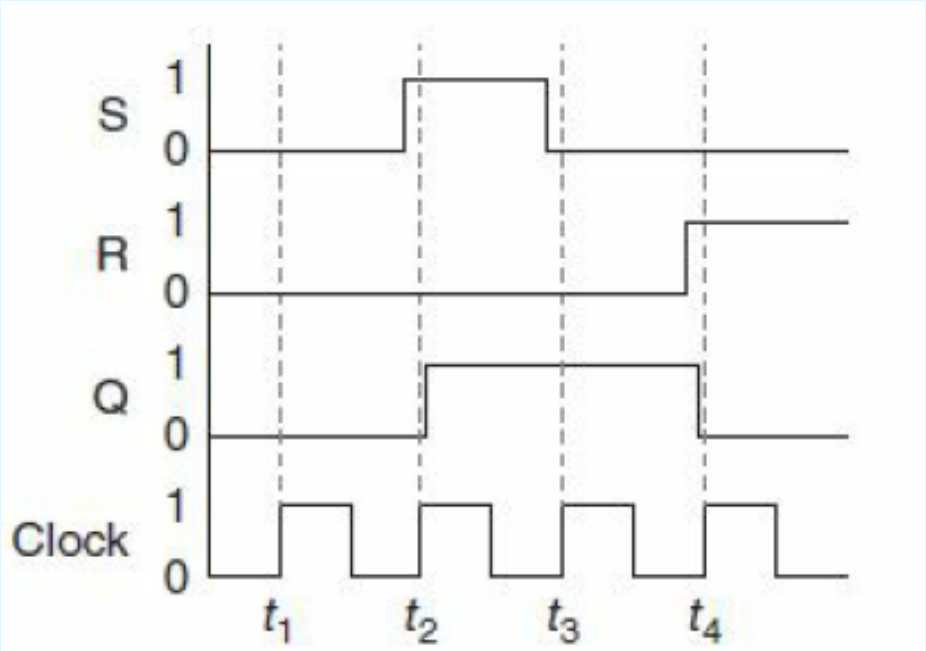


a) SR-latch

S	R	Present State Q(t)	Next State Q(t+1)
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	Undefined
1	1	1	Undefined



a) Clocked SR Flip-Flop



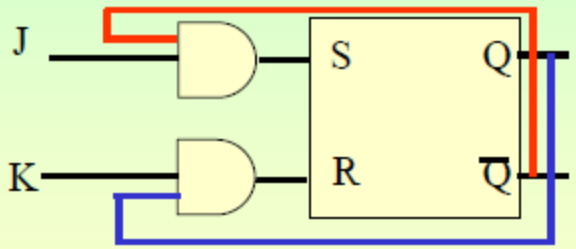
b) Timing Diagram for the SR Flip-Flop
(assuming initial state of Q is 0)

3.6 Sequential Circuits

JK Flip-Flop

- RS Flip-Flop ห้ามไม่ให้ R และ S = 1 พร้อมกัน
- JK Flip-Flop ใช้ได้ทุกเหตุการณ์

J	K	Q
0	0	คงที่ (Latch)
0	1	0
1	0	1
1	1	เปลี่ยนเป็นตรงข้ามกับสถานะเดิม Toggle

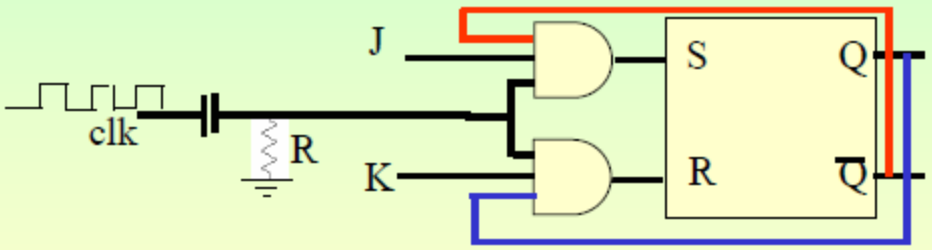


3.6 Sequential Circuits

JK Flip-Flop ที่มีสัญญาณนาฬิกาคุม

- RS Flip-Flop ห้ามไม่ให้ R และ S = 1 พร้อมกัน
- JK Flip-Flop ใช้ได้ทุกเหตุการณ์

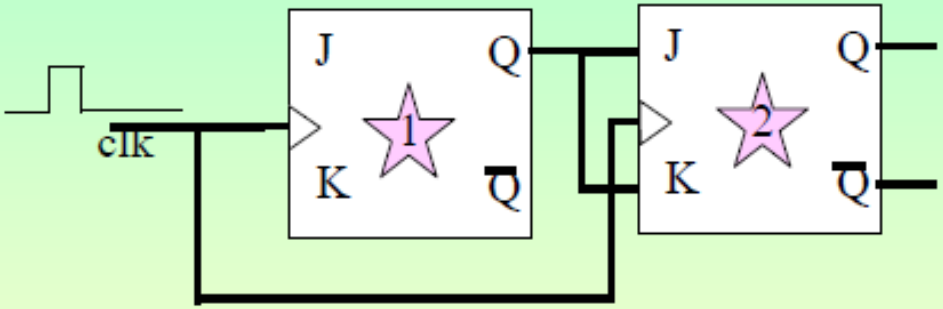
J	K	Q
0	0	คงที่ (Latch)
0	1	0
1	0	1
1	1	เปลี่ยนเป็นตรงข้ามกับสถานะเดิม Toggle



clk = 0 ทำให้ Q มีค่าคงสถานะเดิมตลอด

3.6 Sequential Circuits

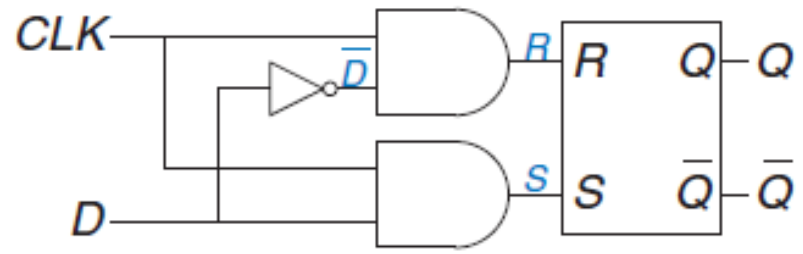
ตัวอย่างวงจร (ต่อ)

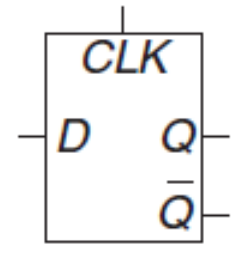


- จากวงจรให้พิจารณาว่าเมื่อ Clock ลูกที่ 1, 2, 3, 4 และ 5 กระตุ้น Q_1, Q_2 แต่ละช่วงมีค่าเท่าไร

3.6 Sequential Circuits

D-Latch



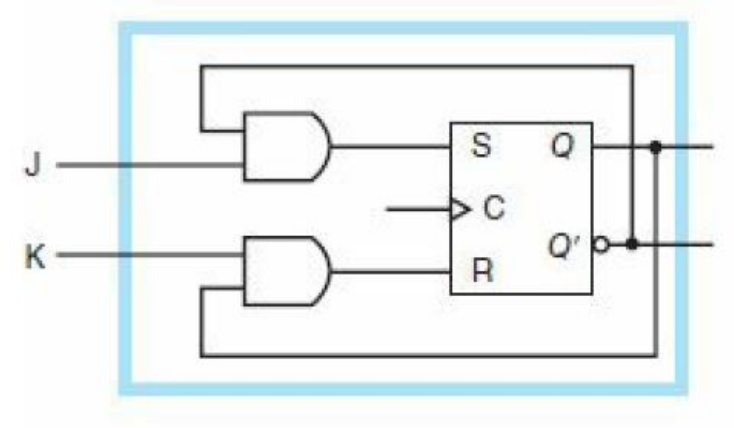


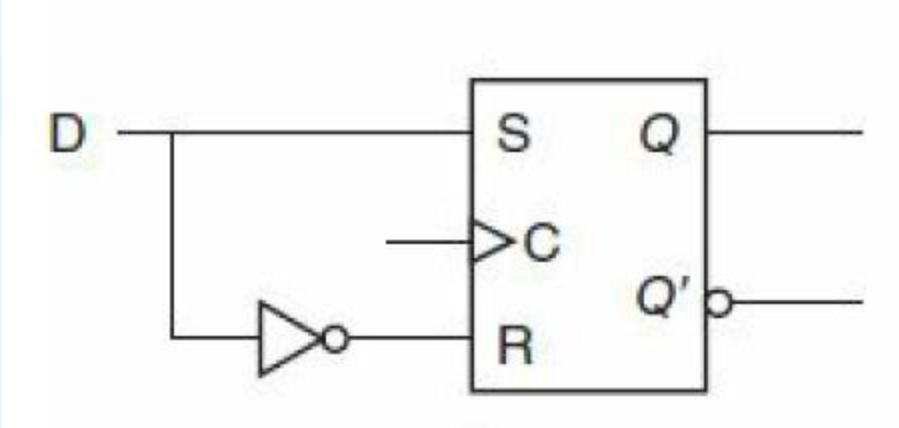
The data input, ***D***, controls what the next state should be.

The clock input, ***CLK***, controls when the state should change.

CLK	D	$\overline{D}$	S	R	Q	$\overline{Q}$
0	X	$\overline{X}$	0	0	Q_{prev}	$\overline{Q}_{prev}$
1	0	1	0	1	0	1
1	1	0	1	0	1	0

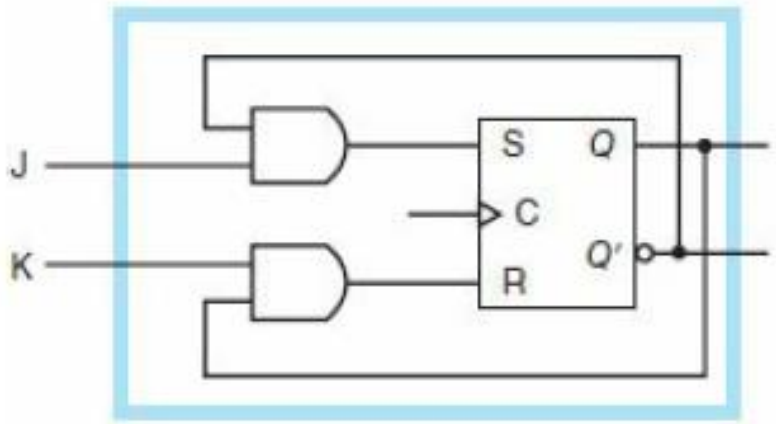
LAB2 Sequential Circuits

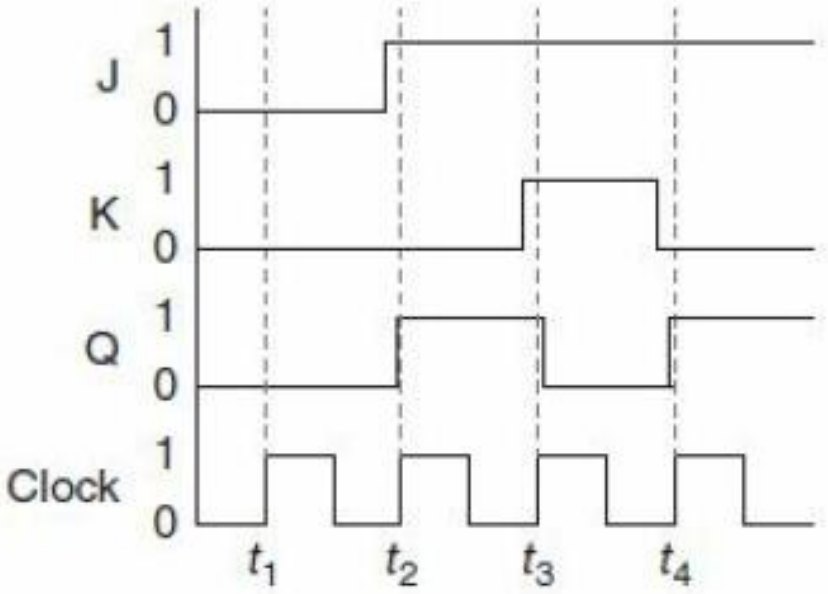




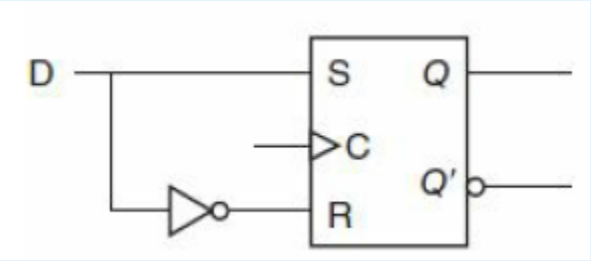
1. จากวงจร JK flip-flop
   - ให้ต่อวงจรให้สร้าง Truth table และ Timing diagram
   - ให้อธิบายการทำงานของวงจรตาม Truth table และ Timing diagram
2. จากวงจร D flip-flop ให้ทำตามขั้นตอนของ JK flip-flop

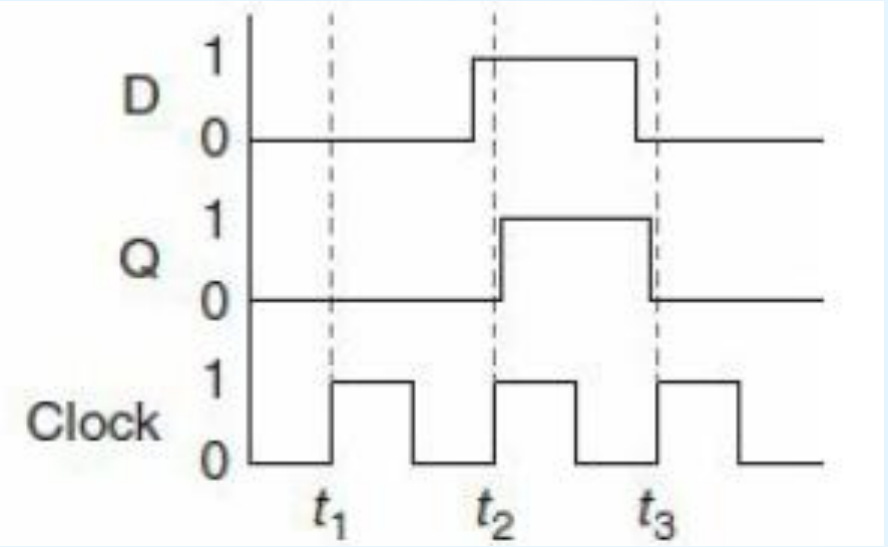
JK Flip-flop





D Flip-flop



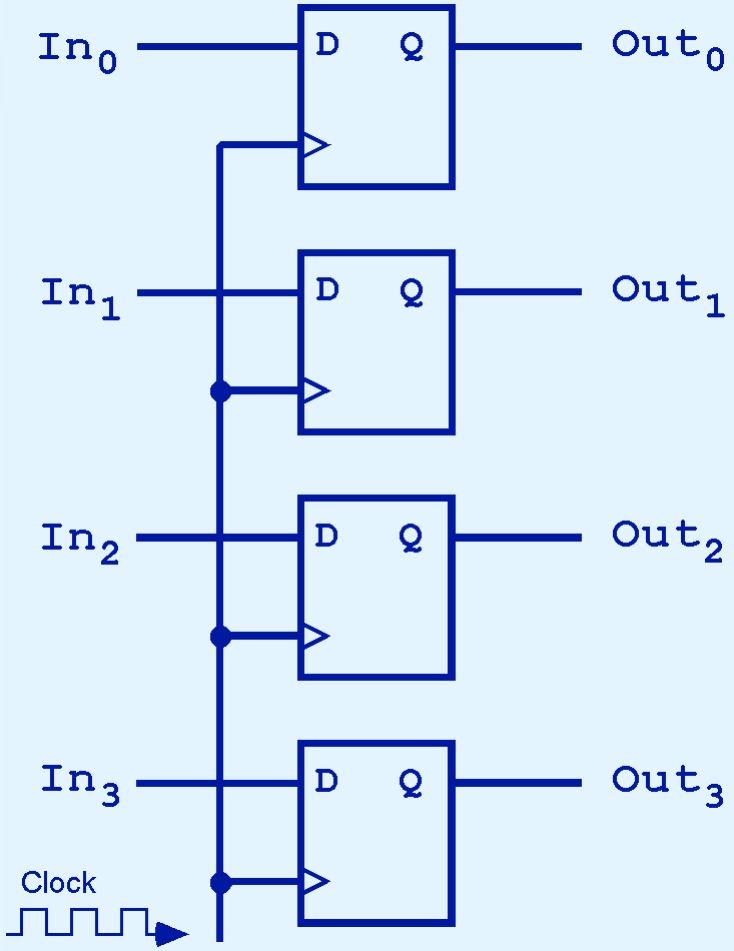


Ex. Sequential Circuits

- Registers,
- counters,
- memories, and
- shift registers

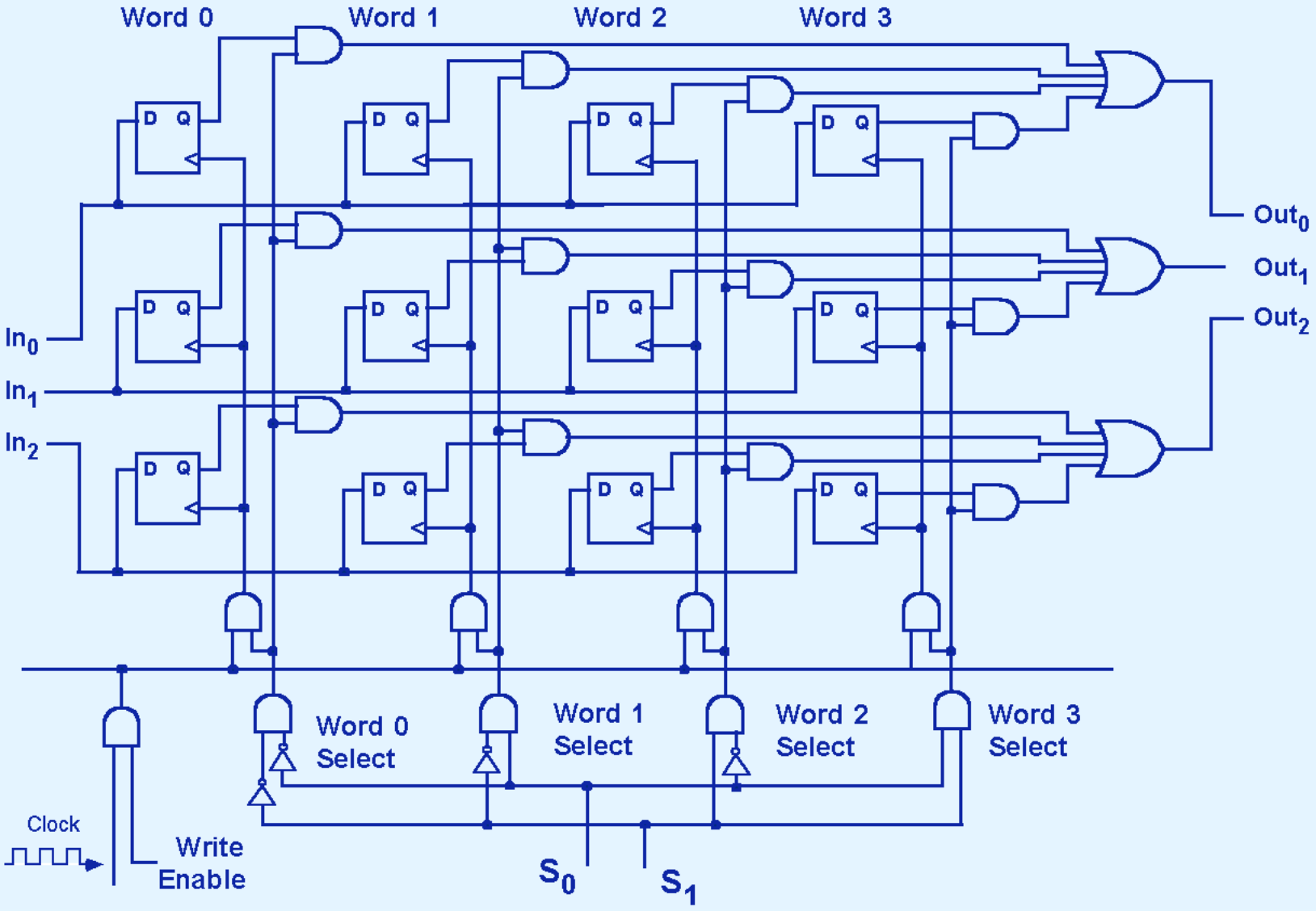
3.6 Sequential Circuits

- 4-bit register consisting of four D flip-flops. You will usually see its block diagram (below) instead.



A larger memory configuration is shown on the next slide.

3.6 Sequential Circuits



3.6 Sequential Circuits

- A binary counter is another example of a sequential circuit.
- The low-order bit is complemented at each clock pulse.
- Whenever it changes from 0 to 1, the next bit is complemented, and so on through the other flip-flops.